REMARKS

Applicants have amended claims 25 and 34 to correct typographical errors. In claim 25 a comma was added on line 2 between "a third clock pin" and "a functional clock pin" and on line 13, "having an first data input" was changed to -- having a first data input --. In claim 34, on line 13, "having an first data input" was changed to -- having a first data input --. The amendments of claims 25 and 34 were not made in response to the Examiners rejection of claims 25 and 34.

The Examiner objected to the claims 25-42 "for containing a plurality of elements or steps which are not separated by a line indent. An amendment is required to put the claim in proper format. Line indents aid in understanding the logical grouping of a claim's elements." In response, Applicants have reviewed the United States Patent Application Publication US2006/0041802 for the present Application and find that the claim steps are separated by line indents. The Examiner should note, that the claims, as presented in this response include line indents between steps and were copied from Applicants original source document. Applicants are thus unable to respond to the Examiners objection. Applicants suggest, that a internal Patent Office software problem or a problem with early Patent Office electronic filing software may be responsible for missing line indents in the Examiners copy.

The Examiner objected to claims 28 and 37 stating "Claim 28 is objected to because of the following informalities: the limitation, 'generate a first B clock pulse' and 'followed by a C clock pulse' does not show which pin it is related to. These limitations should be changed to recite: 'generate a first B clock pulse on said ZB clock output' and 'followed by a C clock pulse on said ZC clock output'. Appropriate correction is required. Claim 37 is objected to because of the following informalities: the phrase 'generating a first B clock pulse' and 'followed by a C clock pulse' does not show which pin it is related to. These limitations should be changed to

recite: 'generating a first B clock pulse on said ZB clock output' and 'followed by a C clock pulse on said ZC clock output' Appropriate correction is required." In response, Applicants have so amended claims 28 and 37.

The Examiner has stated that "claims 26, 28-33, 35 and 37-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and anv intervening claims. However, the claim objections to claims 28 and 37 above must be corrected before they would be allowed.. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

The Examiner rejected claims 25, 27, 34 and 36 under 35 U.S.C. §102(b) as being unpatentable over Lackey (US-6467044).

Applicants respectfully traverse the §102(b) and rejections with the following arguments.

35 USC § 102

The Examiner rejected claims 25 and 34 under 35 U.S.C §102(b) stating "Lackey teaches a test controller **(The clock templates 12 are designed for use in a test controller, Fig. 1, col. 3, ll 36-37)** having a test input connected to said test pin, a first test clock input **(B)** connected to said first test clock pin, a functional clock input connected to said functional clock pin **(oscillator 10 generates system clock, Fig. 1, col. 3,** II. **33-34),** a first control output and a second control output. Lackey also teaches a clock splitter **(clock splitter 50, Fig. 3 and Fig. 5, col. 4, ll 40_60)** having a first clock input **(C clock, Fig. 5)** connected to said second test clock pin, a second clock input connected to said functional clock pin **(System clock, Fig. 5),** a first control input **(Y clock, Fig. 5)** connected to said first control output of said test controller, a second control input **(B clock, Fig. 5)** connected to said second control output and of said controller, an enable input **(LSSD MODE bar, Fig. 5)** connected to said enable pin, a ZB clock output **(Bout, Fig. 5)** and a ZC clock output **(Cout, Fig. 5).** Lackey also teaches an LSSD scan chain **(LSSD latches 52,54 and 56,58, Fig. 3)** comprised of serially connected latches, a first stage of each latch having an first data input **(Data In),** a second data input and a C clock input connected to said ZC clock output of said clock splitter **(Capture Clock),** an A CLK input connected to said third test clock pin, a second stage of each latch having a data output and a B clock input connected to said ZB clock output of said clock splitter (Launch **Clock),** a data output of a previous latch connected to a first input pin of an immediately subsequent latch, a first data input of a first latch of said LSSD scan chain connected to said scan-in pin and a data output pin of a last scan chain latch of said scan chain connected to said scan-out pin."

Applicants contend that claim 25 is not anticipated by Lackey because Lackey does not teach each and every feature of claim 25.

As a first example Lackey does not teach "a first stage of each latch having a first data input, a second data input and a C clock input." Applicants respectfully point out in FIG. 3 of Lackey, the first stages (master 52 and 56) of master/slave latches 52/54 and 56/58 have only a data input (Data In) and a C clock input (Capture Clock). There is no "second data input" as Applicants claim 25 requires.

As a second example, Lackey does not teach or suggest "a first stage of each latch having ... a C clock input connected to said ZC clock output of said clock splitter, an A CLK input connected to said third test clock pin" and "a second stage of each latch having ... a B clock input." Applicants respectfully point out in FIG. 3 of Lackey, there is only one clock input (Capture Clock) in master latches 52 and 56 and only one clock input (Launch Clock) in slave latches 54 and 58. There is no "A CLK input" to "a first stage of each latch" as Applicants claim 25 requires.

As a third example, Lackey does not teach or suggest "a data output of a previous latch connected to a first input pin of an immediately subsequent latch." Applicants respectfully point out in FIG. 3 of Lackey, the Data Out of both slave latches 54 and 58 are shown as inputs to combinational logic 60 and the Data In of both master latches 52 and 54 are shown coming from combinational logic 60. Lackey only teaches in col. 4, lines 47-51 that "Data from combinational logic 60 is applied to 'data in' terminal of the master latches 52, 56. Each of the slave latches 54, 58 generates 'data out' signal and return it to the combinational logic." Thus, there is no teaching in Lackey that the Data Out of slave latch 54 is connected to the Data In of master latch 56.

As a fourth example, Lackey does not teach or suggest "a first data input of a first latch of said LSSD scan chain connected to said scan-in pin and a data output pin of a last scan chain

latch of said scan chain connected to said scan-out pin." Applicants respectfully point out nowhere in Lackey FIG. 3, or anywhere else in Lackey is there is a teaching or even mention of a "scan-in pin" or a "scan-out pin."

As a fifth example, Lackey does not teach or suggest "a clock splitter having a first clock input." Applicants respectfully point out that FIG. 5 is not described in the specification of Lackey. All Lackey teaches about FIG. 5 is found in col. 4, lines 54 and 55 to wit "A person of ordinary skill in the art will easily understand the operation of the logic structures provided in FIGs. 4 and 5." All that Lackey teaches about CLK Y is found in col. 3, lines 19 – 24, which states in part "certain domains are **clocked** at a frequency Y, a frequency less than X .... where frequency Y<frequency X." In col. 3, lines 33-35 in reference to FIG. 1, Lackey states " An oscillator is given with reference number 10, which generates a system clock of frequency X." Thus Y Clock is simply an alternative for System Clock and not a control signal.

Based on the preceding arguments, Applicants respectfully maintain that claim 25 is not unpatentable over Lackey and is in condition for allowance. Since claims 26-33 depend from claim 25, Applicants respectfully maintain that claims 26-33 are likewise in condition for allowance.

Applicants maintain the arguments presented supra with respect to claim 25 are applicable to claim 34 and therefore claim 34 is not unpatentable over Lackey and is in condition for allowance. Since claims 35-42 depend from claim 34, Applicants respectfully maintain that claims 35-42 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR:
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